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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,327	01/27/2006	Kenji Ogawa	MAT-8808US	3515

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EXAMINER	
MCCOMMAS, STUART S	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,327	OGAWA ET AL.	
	Examiner	Art Unit	
	Stuart McCommas	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/8/2008 has been entered.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "the first initialization period" in the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 8 is dependent on claim 7 and is thus rejected for the same reason.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for al all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (United States Patent Application Publication 2002/0021264), hereinafter referenced as Nakamura, in view of Homma (United States Patent Application Publication 2001/0020923), hereinafter referenced as Homma.

Regarding claim 1, Nakamura discloses a method of driving a plasma display panel 15, the plasma display panel including discharge cells 16, each discharge cell formed at an intersection of a scan electrode and a sustain electrode, and a data electrode (figure 3), the method comprising:

dividing one field period into a plurality of sub-fields, each sub-field having an initializing or priming discharge period with an erasure period, a writing period, and sustaining period (figure 9; figure 12);

performing in the priming discharge period and in the erasure period either an all cell initializing operation or a selective initializing operation, where the all-cell initializing operation causes initializing discharge in all the discharge cells for displaying an image (paragraphs 58-63; paragraphs 90-98; figure 8; figure 9; figure 12) and the selective initializing operation selectively causes initializing discharge using the erasure pulse Pe only in the discharge cells where sustaining pulses and sustaining discharge occurred in the previous sub-field (paragraph 63; paragraphs 90-98; figure 9; figure 12).

However Nakamura fails to disclose wherein each of the initializing periods for performing the all-cell initializing operation has an abnormal discharge part which causes self-erasing discharge in the discharge cells having excessive wall charge accumulated therein, the abnormal charge erasing part applying a positive rectangular

waveform voltage, followed by applying a negative rectangular waveform to the scan electrodes.

In a similar field of invention Homma discloses wherein each of the initializing periods for performing the all-cell initializing operation has an abnormal discharge part which causes self-erasing discharge in the discharge cells having excessive wall charge accumulated therein, the abnormal charge erasing part applying a positive rectangular waveform voltage, followed by applying a negative rectangular waveform to the scan electrodes (paragraphs 11-20; paragraphs 61-73; figures 8-10).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura with Homma by specifically providing wherein each of the initializing periods for performing the all-cell initializing operation has an abnormal discharge part which causes self-erasing discharge in the discharge cells having excessive wall charge accumulated therein, the abnormal charge erasing part applying a positive rectangular waveform voltage, followed by applying a negative rectangular waveform to the scan electrodes for the purpose of allowing excess charge to be controlled in a plasma display panel to improve the quality of the display (paragraph 15).

Regarding claim 2, Nakamura and Homma, the combination discloses everything as applied above, further Homma discloses wherein in the abnormal charge erasing part, a voltage is not applied to the sustain electrode when a rectangular waveform voltage with a negative polarity is applied (figures 8-10).

Regarding claim 4, Nakamura and Homma, the combination discloses everything as applied above, further Nakamura discloses wherein a number of times of all-cell initializing period in the one field period is controlled by determining either the all-cell initializing operation or the selective initializing operation according to an APL (paragraphs 90-98; figure 12).

Regarding claim 5, Nakamura and Homma, the combination discloses everything as applied above, further Nakamura discloses wherein a number of times of all-cell initializing period in the one field period is controlled by determining either the all-cell initializing operation or the selective initializing operation according to an APL (paragraphs 90-98; figure 12).

6. Claim 3 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Kim et al. (United States Patent 7,109,951), hereinafter referenced as Kim.

Regarding claim 3, Nakamura discloses a method of driving a plasma display panel 15, the plasma display panel including discharge cells 16, each discharge cell formed at an intersection of a scan electrode and a sustain electrode, and a data electrode (figure 3), the method comprising:

dividing one field period into a plurality of sub-fields, each sub-field having an initializing or priming discharge period with an erasure period, a writing period, and sustaining period (figure 9);

performing in the priming discharge period and in the erasure period either an all cell initializing operation or a selective initializing operation, where the all-cell initializing

operation causes initializing discharge in all the discharge cells for displaying an image (paragraphs 58-63; figure 8; figure 9) and the selective initializing operation selectively causes initializing discharge using the erasure pulse Pe only in the discharge cells where sustaining pulses and sustaining discharge occurred in the previous sub-field (paragraph 63; figure 9). Further Nakamura discloses that each of the initializing periods for performing the all-cell initializing operation has a former half part and a latter half part of the priming discharge period (figure 9), where in the former half part there is application of an ascending ramp waveform voltage Pp to the scan electrodes that causes a first initializing discharge using the scan electrodes as anodes and the sustain electrodes and data electrodes as cathodes (paragraph 60; figure 9) and where in the latter half part, application of a descending ramp waveform voltage Ppe to the scan electrodes causes a second initializing discharge using the scan electrodes as the cathodes and the sustain electrodes and data electrodes as the anodes (paragraph 60; figure 9). Further Nakamura discloses that the initializing period for performing the selective initializing operation has an initializing period for applying a descending ramp waveform voltage to the scan electrodes, using the scan electrodes as the cathodes and the sustain electrodes as the anodes (paragraph 60; figure 9).

However Nakamura fails to disclose an abnormal charge erasing part and, in the abnormal charge erasing part, application of a rectangular waveform voltage to the scan electrodes causes self-erasing discharge in the discharge cells having excessive wall charge accumulated therein.

In a similar field of invention Kim discloses an abnormal discharge part (figure 8), and in the abnormal charge erasing part, application of a rectangular waveform voltage to the scan electrodes causes self-erasing discharge in the discharge cells having excessive wall charge accumulated therein (column 8 lines 64-67; column 9 lines 1-25; figure 8).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura with Kim by specifically providing an abnormal charge erasing part and, in the abnormal charge erasing part, application of a rectangular waveform voltage to the scan electrodes causes self-erasing discharge in the discharge cells having excessive wall charge accumulated therein for the purpose of allowing excess charge to be controlled and erased to avoid misfires in a plasma display panel to improve the quality of the display (column 3 lines 27-41).

Regarding claim 6, Nakamura and Kim, the combination discloses everything as applied above, further Nakamura discloses wherein a number of times of all-cell initializing period in the one field period is controlled by determining either the all-cell initializing operation or the selective initializing operation according to an APL (paragraphs 90-98; figure 12).

Regarding claim 7, Nakamura discloses a method of driving a plasma display panel 15, the plasma display panel including discharge cells 16, each discharge cell formed at an intersection of a scan electrode and a sustain electrode, and a data electrode (figure 3), the method comprising:

dividing one field period into a plurality of sub-fields, each sub-field having an initializing or priming discharge period with an erasure period, a writing period, and sustaining period (figure 9);

in the initializing periods of the plurality of subfields, performing either an all cell initializing operation or a selective initializing operation, where the all-cell initializing operation causes initializing discharge in all the discharge cells for displaying an image (paragraphs 58-63; figure 8; figure 9) and the selective initializing operation selectively causes initializing discharge using the erasure pulse Pe only in the discharge cells where sustaining pulses and sustaining discharge occurred in the previous sub-field (paragraph 63; figure 9). Further Nakamura discloses that each of the initializing periods for performing the all-cell initializing operation has a former half part and a latter half part of the priming discharge period (figure 9), where in the former half part there is application of an ascending ramp waveform voltage Pp to the scan electrodes that causes a first initializing discharge using the scan electrodes as anodes and the sustain electrodes and data electrodes as cathodes (paragraph 60; figure 9) and where in the latter half part, application of a descending ramp waveform voltage Ppe to the scan electrodes causes a second initializing discharge using the scan electrodes as the cathodes and the sustain electrodes and data electrodes as the anodes (paragraph 60; figure 9). Further Nakamura discloses wherein a number of times of all-cell initializing period in the one field period is controlled by determining either the all-cell initializing operation or the selective initializing operation according to an APL (paragraphs 90-98; figure 12).

However Nakamura fails to disclose an abnormal discharge part and a ramp waveform voltage which is ranging from a voltage with the same polarity as the voltage applied during the former half part of the initialization period to a voltage reverse in polarity thereto, and in the abnormal charge erasing part, application of a rectangular waveform voltage, reverse in polarity to the voltage applied during the first initialization period, followed by supplying it with a rectangular waveform voltage reverse in polarity to the scan electrodes.

In a similar field of invention Kim discloses a method and apparatus for driving plasma display panel. In addition, Kim discloses an abnormal discharge part (figure 8) and a ramp waveform voltage which is ranging from a voltage with the same polarity as the voltage applied during the former half part of the initialization period to a voltage reverse in polarity thereto (column 8 lines 36-63; figure 6; figure 8), and in the abnormal charge erasing part, application of a rectangular waveform voltage, reverse in polarity to the voltage applied during the first initialization period (figure 8), followed by supplying it with a rectangular waveform voltage reverse in polarity to a voltage applied during the initialization period (figure 8) to the scan electrodes causes self-erasing discharge in the discharge cells having excessive wall charge accumulated therein (column 8 lines 64-67; column 9 lines 1-25; figure 8).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura by specifically providing an abnormal discharge part and a ramp waveform voltage which is ranging from a voltage with the same polarity as the voltage applied during the former half part of the initialization

period to a voltage reverse in polarity thereto, and in the abnormal charge erasing part, application of a rectangular waveform voltage, reverse in polarity to the voltage applied during the first initialization period, followed by supplying it with a rectangular waveform voltage reverse in polarity to the scan electrodes causes self-erasing discharge in the discharge cells having excessive wall charge accumulated therein for the purpose of allowing excess charge to be controlled and erased to avoid misfires in a plasma display panel to improve the quality of the display (column 3 lines 27-41).

Regarding claim 8, Nakmura and Kim, the combination discloses everything as applied above, further Kim discloses wherein in the abnormal charge erasing part, a voltage is not applied to the sustain electrode when a rectangular waveform voltage is applied (figure 8).

Reponse to Arguments

7. Applicant's arguments with respect to claims 1-8 have been considered but are believed to be answered by and therefore moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stuart McCommas whose telephone number is (571)270-3568. The examiner can normally be reached on Monday-Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571)272-3638. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SSM